EXPEDITED PROCEDURE - EXAMINING GROUP 2816

S/N 09/460,742

PATENT

#13/D(NE) 7/17/02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Rajendran Nair et al.	Examiner: Anh-Quan Tra	
Serial No.:	09/460,742	Group Art Unit: 2816	
Filed:	December 14, 1999	Docket: 884.229US1	
Title:	DEVICE AND METHOD FOR CONTROLLING VOLTAGE VARIATION		

AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.116

Smith 10/9/02 ajr

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Commissioner for Patents
Washington, D.C. 20231

In response to the final office action mailed April 24, 2002, please consider the following remarks.

IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. The substitute claim set is intended to reflect amendment of previously pending claims 4 and 14. The specific amendments to individual claims are detailed in the following marked up set of claims.

do not enter CS 7/18/02

4. [Twice Amended] A circuit comprising:

a voltage node;

a ground node; and

a transistor including a gate, a drain, and a source, the gate being coupled to the voltage node and the drain and source being coupled to the ground node, the transistor operating in the depletion mode, the gate comprising a p-type polysilicon, wherein the transistor has a variable capacitance characteristic that is capable of decreasing noise signals above an absolute value of an operating voltage value at the voltage node and increasing noise signals below the absolute value of the operating voltage value.